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(71) Applicant: **Interuniversitair Micro-Elektronica Centrum (IMEC)**
3001 Heverlee (BE)

(72) Inventors:
- **Collaert, Nadine**
  3052 Blanden (BE)
- **De Meyer, Kristin**
  3020 Herent (BE)

(74) Representative: **Van Malderen, Joelle et al**
Office Van Malderen,
Place Reine Fabiola 6/1
1083 Bruxelles (BE)

(54) FinFET device and a method for manufacturing such device

(57) The present invention is related to a method for forming a FinFET comprising the steps of:

- providing a substrate (1), comprising a semiconductor layer (2),
- forming in said semiconductor layer (2) active areas (4) insulated from each other by field areas (5),
- forming within at least one of said active areas (4) on said semiconductor layer (2) at least one dummy gate (9),
- forming, within said at least one of said active areas (4) and self aligned to said dummy gate (9), source (6) and drain (7) regions in said semiconductor layer (2),
- covering said substrate (1) with an insulating layer (16) leaving said dummy gate (9) exposed,
- forming an open cavity (25) in said insulating layer (16) and in said semiconductor layer (2) by patterning said dummy gate (9) and said semiconductor layer (2) to form respectively a dummy fin (19) and a semiconductor fin (17) aligned to said dummy fin (19), both fins (17), (19) extending from the source (6) to the drain (7) of said at least one active area (4), thereby exposing said semiconductor layer (2)

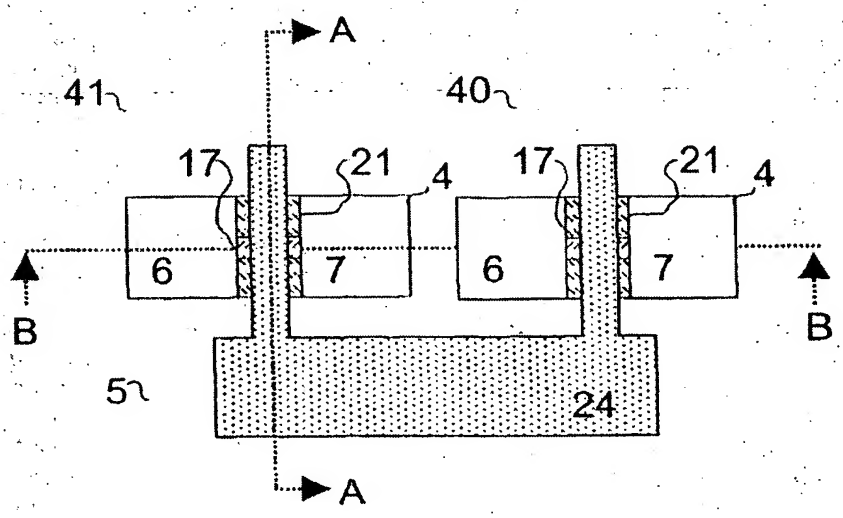

FIG. 1

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Description

Field of the invention

[0001] The present invention generally relates to so-called fin field effect transistors (FET) integrated in a full complementary metal-oxide-semiconductor (CMOS) device process flow. More particularly this invention relates to the integration in such a full CMOS process flow of n-type FinFETs and/or p-type FinFETs having a channel length of 100 nanometer or less.

General description of the background of the invention

[0002] Today's state-of-the-art semiconductor chips feature technology nodes of 0.18 micron (180 nanometers) with 0.13 micron (130 nanometers) technologies just beginning to reach the marketplace. Now the industry plans to deliver 90 nanometers in 2004, 65 nanometers in 2007, 45 nanometers in 2010, 32 nanometers in 2013 and 22 nanometers in 2016. This 2001 schedule, as set forward in the International Technology Roadmap for Semiconductors (ITRS) defined by the Semiconductor Industry Association (SIA), translates to smaller chip dimensions earlier in time than previously thought. Among the main transistor scaling issues to be solved are the need for thinner gate oxides resulting in a higher on-current and hence increased switching speed, a smaller off-current and lower threshold voltage to allow such gate oxide scaling and the use of lower supply voltages, a higher channel mobility and smaller series resistance of the source/drain regions. In order to meet the stringent scaling requirements of this forecast, non-classical CMOS devices and novel materials, such as metal gate materials and high-k gate dielectrics, are currently under investigation.

[0003] One of these non-classical CMOS devices is the so-called FinFET, where the gate envelops at least partially the channel region, contrary to the classic planar device where the gate electrode is formed in one plane on top of the channel region, which is part of the substrate. This substrate further comprises the source and drain regions adjacent to the channel region. The idea of making a double gate transistor by using the sidewalls of a dry-etched silicon (Si) fin as conducting channels was published in 1998 by D. Hisamoto et al. in "A folded-channel MOSFET for deep-sub-tenth Micron Era" in the IEDM Technical Digest 1998 pp 1032-1034. In the Fin FET a thin gate line straddled a thin silicon channel fin. The fabrication process was not optimized and was meant solely for single device demonstration. The proposed process included the use of inside spacers, which could decrease the gate length beyond the lithographical limits. However, the process had some severe drawbacks. It didn't allow the manufacturing of CMOS devices because poly SiGe was used to form the source/drain regions for the pMOS device while poly Si was used to form the source/drain regions of the nMOS device. The final device was assembled by subsequently forming the fin channel, the gate and the source/drain regions. The source/drain areas were not aligned to the gate. The proposed process also didn't allow the integration of SOI CMOS FinFET with SOI BiCMOS.

[0004] Other fabrication processes, reported in literature, include many variations of one basic fabrication process called the "quasi planar" FINFET. Choi et al describe such an alternative in "sub 20-nm CMOS FinFET technologies", IEDM Technical Digest 2001, pp 421-424. This alternative is based on "spacer" lithography: the pattern of the masking Phosphorous-doped Silicon Glass (PSG) spacers is transferred to the underlying Silicon-On-Insulator (SOI) layer thereby having the width of the silicon fins corresponding to the width of the masking spacers. The process only allows submicron fins with a single width as determined by the PSG layer thickness. In this underlying silicon layer source/drain regions can be patterned using conventional lithographic processing. Instead of using this "spacer" lithography alternatives are known using e-beam lithography to pattern the silicon fin channels. Such a FinFET device is described in details in "High-performance symmetric-gate and CMOS compatible V_t asymmetric-gate FinFET devices" in IEDM technical digest 2001 pp437-440, by J. Kedzierski et al. An example of such a device is reproduced in the following drawings, wherein the source/drain regions or pads, as they are labelled there, are formed together with the fin channel in the SOI layer using optical lithography and a hard mask trimming technique. These "quasi planar" FinFET type of processes could allow the formation of CMOS devices. In most alternatives the source/drain areas are not aligned to the gate. As all the silicon of the SOI layer outside the source/drain pads and the fin area is removed, the devices are reciprocally insulated afterwards by forming a planarised oxide layer over the individual devices. The leakage at the edges of this mesa isolation however might degrade device performance. These "quasi planar" FinFET type of processes don't allow the incorporation of metal gates and high-k gate dielectrics easily. Especially the use of metal gates is important for CMOS devices since tuning of the gate workfunction by choosing the appropriate gate electrode material is probably the only way to tune the threshold voltage and thus the device performance.

[0005] In US6252284 a planarised fin device is disclosed. The inventors proposes a complex process schema comprising the steps of first forming the fin, polishing the fin until its desired height is reached, depositing and patterning the gate dielectric and electrode as to cross the fin, forming a silicide on the exposed regions of the fin, forming source/drain areas by depositing a polysilicon layer over the crossing of fin and gate and polishing this deposited polysilicon layer down to the level of the gate electrode followed by an etch-back of

the polished polysilicon layer below the level of the gate electrode, forming a silicide on the exposed surface of the gate electrode. The proposed process flow is very unlikely to be combinable with classical CMOS processing as it requires a large number of additional process steps in an order that is at some points reverse to classical CMOS processing.

Aims of the invention

[0006] The aim of the invention is to offer a double or triple gate semiconductor device, manufactured in a cost effective way. The device according to the invention is in the submicron range or less. The device is a CMOS or BiCMOS device.

[0007] Another aim of the invention is to offer a submicron FinFET that can be formed in combination with standard CMOS and/or BiCMOS devices. The devices according to the present invention overcome the deficiencies of the prior art such as short channel effects, leakage, lack of integratibility, lack of sufficient lateral isolation between the devices.

[0008] Another aim of the invention is to disclose a method for manufacturing such devices. These methods allow the full integration of devices according to the present invention with standard planar CMOS and/or BiCMOS devices in an easy and cost-efficient way with a minimal number of additional process steps. These methods also allow the use of high-k gate dielectric and metal gate electrode within the devices of invention.

Summary of the invention

[0009] In one embodiment of the present invention at least one FinFET device is manufactured in a CMOS compatible way.

[0010] In a semiconductor layer on a substrate active areas are formed, insulated by field regions. On these active areas at least one dummy gate is formed by depositing a layer or stack of layers and patterning this layer or stack of layers. Self aligned to and spaced apart by the dummy gate source and drain regions are incorporated in the semiconductor layer. The substrate is covered with a dielectric leaving only the dummy gate exposed. The exposed dummy gate is patterned to create a cavity spacing apart the source and drain regions. Spacers are formed against the sides of the cavity to cover the exposed sidewalls of the source and drain regions. The patterning of the dummy gate yields a dummy fin in the cavity extending from the source and drain region. This dummy fin is used to pattern the underlying semiconductor layer yielding a semiconductor fin connecting the source and the drain. The dummy fin can be completely removed to from a triple gate device, whereby the gate dielectric has substantial the same thickness when straddling the semiconductor fin. If the dummy fin is only partially thinned a double gate device is formed, whereby a thinner gate dielectric couples the gate electrode to the semiconductor fin at the sidewalls, while the remaining dummy fin on top of the semiconductor fin isolates the gate electrode from the top surface of the semiconductor fin.

[0011] In another embodiment of the present invention classical planar CMOS or BiCMOS devices can be formed in an integrated way with a FinFET device according to the present invention.

[0012] When using the above process sequence planar CMOS or BiCMOS devices can be made while manufacturing the FinFET device. On some active areas FinFET devices can be formed while on other active areas planar MOS devices can be formed. If the dummy gate comprises a conductive layer, e.g. polysilicon, on top of a dielectric layer, e.g. siliconoxide, this dummy gate can serve as the gate of a planar device. The patterning of the dummy layer in order to form the dummy gate includes then patterning the dummy layers in order to form the planar gate. Ion implantation steps can be formed self-aligned to dummy gate and planar gate to form the source and drain regions of both type of devices. Spacers can be formed against the dummy gate and planar gate as is common practice in planar CMOS technology. After covering the substrate with a planarizing dielectric leaving only the dummy gate exposed, the planar gate remains unaffected and is protected during further processing, e.g. by applying only masked removal steps. In case of replacement gate devices the dummy gate is not patterned to form the fin but is completely removed because a replacement gate device differs from the classic planar device in that the high-k dielectric and/or metal gate is formed after forming the device structure.

[0013] In another embodiment of the invention high-k dielectrics and/or metal conductor are introduced to form a FinFET device with the desired electrical characteristics. The proposed sequence allows the use of high-k dielectrics as gate dielectrics or metals as gate electrode material, because first the device structure is formed and covered with a protective dielectric only leaving the dummy gate exposed. When depositing the high-k dielectric and/or a metal gate layer these layers are only in contact with the channel part of the semiconductor fin.

[0014] In another embodiment a CMOS circuit described. This CMOS circuit comprises at least two active areas formed in a semiconductor layer, said at least two active areas are insulated from each other by field regions. Each of said active areas comprises at least one FinFET device. Each of said FinFET devices comprises a source and a drain area formed in said semiconductor layer, and a spacing in between, and a semiconductor fin formed in the same semiconductor layer and extending in said spacing from said source to said drain. An insulating oxide covers said CMOS circuit outside said spacing, and spacers are formed against the sidewalls of said spacing. The CMOS circuit further comprises a stack of a gate dielectric and a gate electrode overlap-

ping said semiconductor fin. Preferably the gate dielectric comprises a high-k dielectric. Optionally the gate electrode comprises a metal. The stack of gate dielectric and gate electrode can be patterned to extend beyond said spacing or can be planarized to only fill the cavity in between the source and drain region. The CMOS circuit can further comprise at least one active area comprising at least one planar FET device.

Short description of the drawings

[0015] All drawings are intended to illustrate some aspects and embodiments of the present invention. Devices are depicted in a simplified way for reason of clarity. Not all alternatives and options are shown and therefore the invention is not limited to the content of the given drawings. Like numerals are employed to reference like parts in the different figures.

[0016] Figure 1 shows a top view of a CMOS invertor circuit according to the present invention.

[0017] Figures 2a and 2b show respectively the cross sections AA and BB of figure 1 after patterning the dummy gate stack. Figure 2c shows the top view of figure 2b.

[0018] Figures 3a and 3b show respectively the cross sections AA and BB of figure 1 after patterning polishing the insulating dielectric.

[0019] Figures 4a, 4b and 4c show respectively the cross sections AA and BB of figure 1 after patterning the dummy gate stack. Figure 4d shows the top view of figure 4c.

[0020] Figures 5a and 5b show respectively the cross sections AA and BB of figure 1 after partially removing the patterned dummy gate stack.

[0021] Figures 6a and 6b show respectively the cross sections AA and BB of figure 1 after forming the inside spacers. Figure 6c shows the top view of figure 6b.

[0022] Figures 7a and 7b show respectively the cross sections AA and BB of figure 1 after patterning the dummy gate stack and removing the dummy gate layers.

[0023] Figures 8a and 8b show respectively the cross sections AA and BB of figure 1 after etching the gate electrode.

[0024] Figures 9a and 9b show respectively the cross sections AA and BB of figure 1 after planarizing the gate electrode.

Detailed description of preferred embodiments of the present invention

[0025] In relation to the appended drawings the present invention is described in detail in the sequel. It is apparent however that a person skilled in the art can imagine several other equivalent embodiments or other ways of executing the present invention, the spirit and scope of the present invention being limited only by the terms of the appended claims.

[0026] The double or triple gate MOSFET is considered as the most promising device architecture for scaling CMOS into the deep sub-100 nm regime. Improved short channel effects and current drive capability are important features of this device. The fabrication of this device architecture is not straightforward and several attempts have been made to fabricate these devices in an economically acceptable way. As already outlined in the prior art section a variety in double gate devices exist and there are different process sequences for manufacturing such double gate MOSFET's each sequence having its associated advantages and disadvantages. Hence the particular order and specific steps in each process are critical to describe the fabrication of a particular device. Altering a step or sequence in a process flow may therefore result in a MOSFET or CMOS device with different characteristics.

[0027] For the purpose of teaching the invention the process for forming a CMOS invertor circuit will be outlined. Figure 1 shows a top view of the CMOS invertor according to the present invention. The field oxide region 5 isolates the active areas 4 in which respectively the nMOS device 40 and the pMOS 41 device of the CMOS invertor are formed. Both devices have the gate electrode 22 in common. This gate electrode 22 straddles the semiconductor fin 16 connecting the source 6 and the drain 7 of the MOSFET. The semiconductor fin 16, the source 6 and the drain 7 area of the transistors are formed in the same, continuous, layer 2 (not indicated). Against the sidewalls of the area 8 (not indicated) inside the active area 4 and outlined by the source 6, the drain 7 and the field region 5, sidewall spacers 20 are formed. These sidewall spacers are formed 20a in this region 8 adjacent to the semiconductor fin 16, and above 20b the semiconductor fin 16 thereby offsetting the gate electrode 22 from the edges of the source 6 and drain 7 regions. Cross sectional drawings of this invertor will be used to illustrate various process steps. In figures "a" the section AA made along the channel of a MOSFET is shown while in figures "b" the section BB along the fin perpendicular to section AA is shown.

[0028] The processing starts with a substrate 1. Typically this substrate 1 is a semiconductor substrate such as a silicon or germanium wafer. In a preferred embodiment this substrate is a Silicon-On-Insulator (SOI) wafer 1, with a top layer of silicon 2 upon an underlying oxide layer 3. However a semiconductor wafer 1 can be used on which only locally SOI regions are created by e.g. only forming a stack of a semiconductor layer 2 on top of a dielectric layer 3 on top of the substrate 1 in selected areas. This stack can be obtained for example by locally forming the dielectric layer 3 in the selected areas,e .g. by growing an oxide, and then locally forming the semiconductor layer 2 on this dielectric layer 3, e.g. by selective atomic layer CVD, as appreciated by a person skilled in the art. Within these selected areas devices according to the present invention are formed while in the non-selected areas, i.e. the non-SOI regions, classical bulk planar CMOS devices can be made in this substrate 1. A person skilled in the art will understand

that for a bulk FET the channel region or at least the space charge region of the channel area formed during operation of the device will extend into the bulk of the semiconductor substrate 1, whereas in case of a SOI device a dielectric layer 3 separates the device layer 2 from the bulk of the substrate 1. For the purpose of teaching the invention an SOI wafer is used as starting substrate. In the semiconductor top layer 2 active area regions 4 are defined by forming field regions 5 that laterally isolate these active area regions 4. Later on in the processing transistors will be formed within the perimeter of these active area regions 4. The field regions 5 can be created using standard isolation methods, such as growing a field oxide or forming trenches in the substrate 1 filled with a dielectric as is known in the shallow trench isolation (STI) method, while protecting the active area regions 4 with a nitride masking layer. Appropriate doping of the active area regions 4 can be done to result in the desired doping profiles within the semiconductor layer 2. For example pwell and nwell regions for respectively receiving the nMOS and pMOS devices are formed by doping the active area regions 4 using e.g. ion implantation of boron and phosphorous respectively. In some of the thus formed active area's FinFETs according planar CMOS and/or BiCMOS devices can be formed. As will be clear from the description the present invention allows to combine the formation of FinFET devices with classical planar devices without impacting the processing of these standard planar devices.

[0029] Within each active area 4 that is selected to have a FinFET 40,41 to be formed therein, a source region 6, a drain region 7 and a gate region 8 are outlined by forming a dummy gate structure 9 on top of this selected active areas as shown in figure 2c. The source 6 and drain 7 region are abutted by and aligned to this dummy gate structure 9, whereas the gate region 8, i.e. the region in between and separating the source 6 and drain 7 region, is covered by this dummy gate structure 9. The dummy gate structure 9 can comprise a single layer or a stack of layers whatever is appropriate. The dummy gate structure 9 can be formed using conventional semiconductor processing techniques, such as thermally growing an oxide 10 on top of the active area region 4 followed by a conformal deposition, e.g. by means of Chemical Vapor Deposition (CVD) process, of a top layer 11. This layer 11 can comprise a polysilicon 12 and/or a nitride layer 13. The deposited layers, in the example of a dual gate device being nitride 13 on top of polysilicon 12 on top of an oxide layer 10, are then patterned to yield the dummy gate structure 9. Preferably the step of patterning the dummy gate stack 9 uses optical lithography and dry etching. One purpose of this dummy gate structure 9 is to determine the lateral spacing "s" between the source 6 and drain 7 region, hence a more relaxed lithographic technology can be used for this patterning step. For example 248nm or 193nm DUV technologies, which are used to define dimensions in the range of 100 to 400 nanometer in the photosensitive resist layer, can be applied. The dummy gate structure 9 will be removed later on in the process sequence and is at this stage in the process sequence only used to space apart the source 7 and drain 8 area. One requirement of the material or materials composing the dummy gate structure 9 is the ability to remove this material or these materials selective to the underlying layers or surrounding layer. In the example given above the nitride layer 13 is selectively removable with respect to the polysilicon layer 12 of the dummy gate 9. This polysilicon layer 12 in its turn can be removed selective to the underlying oxide layer 10 using a dry etch process, while on its turn this oxide layer 10 of the dummy gate 9 can be removed selective to the semiconductor material 2 by wet etching the oxide employing an HF-based solution. Other materials know to a person skilled in the art can be used to form the dummy gate structure 9. Another requirement of the dummy gate 9 is that the layer 11 or at least the top part 13 of this layer 11 can be used as a polish stop layer when planarising the semiconductor using Chemical Mechanical Polishing (CMP).

[0030] The standard CMOS devices, not shown in the drawings, formed on active areas 4 other than the active areas 4 in which the devices according to the present invention are formed, can use this oxide 10 as the gate dielectric and this polysilicon layer 12 as the gate electrode layer. Patterning the dummy gate 9 also includes then patterning the gate stack of the planar CMOS devices. Preferably dedicated gate dielectric and gate electrode layers are formed for these classical CMOS devices in which case the layers (10,11) used to form the dummy gate stack 9 are only applied to make the FinFET according to the present invention. This dummy gate stack 9 can also serve as a dummy gate stack in order to create replacement gate devices. United States patent US 2001 0049183 A1, hereby incorporated by reference in its entirety, illustrates methods for forming such replacement gate devices.

[0031] Figure 2a and 2b shows the cross sections AA and BB of the invertor after the patterning of the dummy gate 9 of the nMOS 40 and pMOS 41 transistor. It is obvious for a person skilled in the art that the alignment of the dummy gate 9 as shown in figure 2a is a theoretical example whereas in processing the dummy gate 9 might overlap on the field regions 5 as to compensate for misalignment errors.

[0032] If a thin film SOI wafer is used as starting substrate 1 the initial thickness of the thin SOI layer 2 might result in a very high series resistance within the finished transistor or might impede the growth of a silicide layer on the source 6 and drain 7 areas. For these and other reasons the thickness of the SOI layer 2 within the source 6 and drain 7 areas can be increased resulting in so-called elevated source and drain regions. In a preferred embodiment the height of the silicon layer in the source 6 and drain 7 regions is increased by epitaxially growing a silicon layer 14 selective on the exposed silicon starting substrate 2. As the dummy gate structure

9 is still present during this epitaxial growth step only the source 6 and drain 7 regions are exposed while the gate region 8 is protected and covered by the dummy gate 9. The material or materials used for the dummy gate 9, or at least for the parts of the dummy gate 9 that are exposed during this growth step, must also be chosen to not allow any substantial growth of semiconductor material on them during the step of forming elevated source and drain areas. The dummy gate 9 masks the gate area 8 during the step of selectively growing semiconductor material in the exposed source 6 and drain 7 regions.

[0033] The source 6 and drain regions 7 are doped to obtain n- or p-type source and drain junctions with the desired doping profile for respectively the nMOS 40 and pMOS 41 transistor. Preferably ion implantation is used to create a Highly Doped Drain (HDD) profile within the source 6 and drain regions 7. The doping profile is preferably uniform within the source 6 and drain 7 regions both in lateral as well as in vertical direction resulting in a uniform electrical current flow from the junctions 6,7 towards the gate area 8. As the dummy gate structure 9 is still present during the step of implanting the source 6 and drain 7 regions the doping of the exposed source 6 and drain 7 regions is self-aligned to this dummy gate structure 9. Incorporating of the dopants within the source 6 and drain 7 regions of the FinFET devices according to the present invention can be done simultaneously with doping their counterparts of the planar MOS devices.

[0034] Optionally a silicide 15, e.g. $TiSi_2$, $CoSi_2$, can be formed on the source 6 and drain 7 areas prior to the step of covering the substrate surface with a dielectric layer. Methods for forming silicides are known to persons skilled in the art. The dummy gate 9 allows forming selectively silicides on the exposed source 6 and drain 7 areas.

[0035] A dielectric layer or stack of layers 16 is formed over the substrate comprising the field regions 5 and the active area regions 4 which comprise doped source 6 regions, doped drain 7 regions and the dummy gate structure 9 which covers the gate region 8. This dielectric layer 16 is sometimes referred to as the premetal dielectric (PMD) as it concludes in conventional CMOS processing the front end processing of the active devices being the planar CMOS and/or BiCMOS transistors. In a preferred embodiment this dielectric layer 16 is an oxide or oxide-like layer formed using CVD processes, such as plasma-enhanced CVD. After forming this planarising dielectric 16 the substrate is polished, layer 11 of the dummy gate structure 9 is substantially exposed. This planarization by CMP will provide a surface having topography typically within 10 to 5%. The top layer 11 of the dummy gate 9 will act as a polish-stop layer during this polishing step in order to have a polishing process that uses endpoint detection rather than a timed polishing step. During this step only the dummy gates 9 are exposed while the remainder of the substrate is covered with the dielectric 16. Figure 3a and 3b shows the cross sections AA and BB of the invertor after polishing of the insulating dielectric 16 and exposure of the top surface of the dummy gate 9. The active areas in which the classical planar devices are made, preferably remains covered with the insulating dielectric 16.

[0036] After forming the lateral isolation 5 of the active areas 4 and planarizing the dielectric 16 covering the substrate 1 thereby exposing the top layer 11 of the dummy gate 9, the fin-part of the FinFET will be defined. In the active areas 4 in which FinFETs will be formed, patterning of the homogeneous semiconductor layer 2 is done to yield a semiconductor fin 17 having the desired cross sectional width "w". The semiconductor fin connects the source 6 and drain 7 regions. In other active areas where a dummy gate structure is still present but where replacement gate MOSFETs are to be formed, this additional patterning step will be omitted because the dummy gate will here be completely removed, while in some active area's classical devices are formed without dummy gate and hence this patterning step is also obsolete in these areas.

[0037] In the course of the proposed process flow the dummy layers 10 and 11 which optionally comprises layers 12,13, that constitute the dummy gate stack 9, are patterned twice to finally form the semiconductor fin 17. In a first pattering step the dummy gate 9 is formed to outline and to separate and space apart the source 6 and drain 7 regions. The spacing "s" between the source 6 and drain 7 regions corresponds to the length of the semiconductor fin 17. The second patterning step that is now introduced, defines the, cross-sectional, width "w" of the fin 17 orthogonal to the spacing "s". The dummy gate 9 and the semiconductor film 2 underneath it are patterned to define the fin 18 which comprises a top element 19 formed in the dummy stack materials, e.g. oxide 10 and polysilicon 12 and/or nitride 13 and a bottom element 17 which is the semiconductor fin. The selective removal of the exposed dummy gate stack 9 and the underlying semiconductor material 2 can be done in a single step. Both the exposed parts of the dummy gate 9 and the semiconductor material 2 are then removed using the resist pattern as a masking layer. Figure 4a shows the cross section AA in case the dummy gate 9 and the underlying semiconductor layer 2 are patterned in a single step, self aligned to each other, to create an open cavity 25 in which respectively the dummy fin 19 and the semiconductor fin 17 are present. The selective removal of the exposed dummy gate stack 9 and the underlying semiconductor material 2 can also be done in a two-step process. First the dummy gate 9 is patterned to yield the top element 19 using the resist pattern as a masking layer as shown in figure 4b. By patterning the dummy gate a part of the open cavity 25 is now created in the dielectric 16 whose dimensions correspond to these of the dummy gate 9. Within this cavity a dummy pattern 18 remains extending from the source to the drain. After removing this patterned resist layer the pat-

terned dummy gate stack or dummy fin 19 serves as a hardmask for the etching selfaligned to the dummy fin 19 the semiconductor film 2 to yield the semiconductor fin 17. In this second etching step the partially formed open cavity 25 is extended from the planarized dielectric 16 into the underlying semiconductor layer 2 to finally yield the complete open cavity 25 separating the source 6 and drain 7 area.. The patterning of the fin 18 can be done using any lithographic technology. For example photolithographic technologies such as 248nm or 193nm DUV technology, which are used to define dimensions in the range of 100 to 400 nanometer in the photosensitive resist layer, can be applied. In a preferred embodiment of the invention e-beam lithography is applied to define dimensions in the photosensitive resist layer of 100nm or less, typically 50nm or less. The thus formed resist pattern then masks the underlying layer or layers during the subsequent etching step Preferably this etching step is a dry etching step because sub 100nm features are to be formed in the dummy gate stack 9 and in the underlying semiconductor material 2. Figure 4a shows the cross sectional view AA of the invertor circuit after the dummy and semiconductor fin patterned and before the dummy fin 19 is at least partially removed. Figure 4b shows the cross sectional view AA of the invertor circuit after the dummy fin 19 is patterned. Figure 4c shows a cross sectional view BB of figure 4a. Figure 4d is a top view of the invertor circuit at this stage of the processing. The substrate 1 is covered with the dielectric 16. Only the cavity 25 between the source 6 and drain 7 region is exposed. Within this cavity 25 the fin 17 (only the dummy fin 19 is visible in figure 4c) extends from the source side to the drain side. For the purpose of teaching the perimeter of the active area 4 is indicated by a dashed line in figure 4d. At this stage of the processing the cavity 25 is not filled. As can be seen in figure 4d source 6, drain 7 and the semiconductor fin 17 underneath the dummy fin 19 are formed in the same semiconductor layer 2. Both source 6 and drain 7 stretch out on the left and on the right side of the semiconductor fin 17. Because the width of source 6 and drain 7 region is larger than the width of the semiconductor fin 2, contacting of the source 6 and drain 7 during the back-end-of-line processing is made easier.

[0038] In case of double gate devices, the dummy fin 19 is partly removed. As shown in figures 5a and 5b a top part 13 of the patterned dummy gate stack 19 is removed to have the surface of the fin 18 below the level of the planarized dielectric 16. In figure 5a the dashed square show the removed part 13 of the dummy fin 19 whereby the as-deposited thickness d is reduced to the thickness d'. In the example given the nitride part 13 is selectively removed and the polysilicon part 12 is exposed. In case of triple gate devices the complete dummy fin 19 on top of the patterned semiconductor film 17 is selectively removed thereby exposing not only the sides but also the top surface of the semiconductor fin 17 as shown in figures 7a and 7b.

[0039] After patterning the semiconductor fin 17 and lowering the surface of the fin 18 below the level of the planarizing dielectric 16, a short thermal oxidation can be performed to oxidize the exposed surfaces of the semiconductor fin 17. The thus-formed sacrificial oxide will be removed using a wet etching step, e.g. a HF-based solution. This sequence of thermally oxidizing and wet etching of the thus formed oxide will remove the etch damage from the surface of the semiconductor fin 17. The width "w" of the semiconductor fin 17 can also be reduced, as a controlled part, i.e. the oxidezed part, of the semiconductor fin 17 will be removed thereby thinning the semiconductor fin 17 below its lithographic defined width.

[0040] At this stage in the processing in the selected active area regions 4 a monolithic structure is present comprising a homogeneous semiconductor layer 2 in which a doped source 6 and drain regions 7 and a semiconductor fin 17 in between are formed. A dielectric layer 14 covers this monolithic structure only exposing the spacing 8 between the source 6 and drain 7 region. Within this cavity having lateral dimensions corresponding to the spacing 8 the fin 18 having lateral dimensions "s" and "w" connects the source 6 and the drain 7.

[0041] Sidewall spacers are now formed against the side walls of the cavity formed in the dielectric 16 and the semiconductor layer 2. A dielectric layer 20 typically nitride, or a stack of layers, is deposited in a uniform way over the surface of the substrate, followed by anisotropically etching, e.g. dry etching, this dielectric layer 20 to form spacers 21. This etching step creates spacers against the walls of the cavity also on top of the lowered fin 18. No spacers 21 are formed on the sides of the fin 17. So the sides of the fin, including the sides of the semiconductor fin 16, are essentially free from the spacer dielectric 20 and remain exposed. These inside spacers 21 hence overlap the sidewalls of the source 6 and drain regions 7 adjacent to the fin 17 and form an insulating layer over these sidewalls. On the top surface of the fin 17 adjacent to the source 6 and drain 7 region also spacers 21 are formed. At this stage of the processing the source and drain regions are wrapped by dielectric material: in lateral direction at three sides by the field 5 dielectric surrounding the active area 4 and by the sidewall spacers 21, in vertical direction by the planarising dielectric 16 and by the oxide layer 3. The height of this inside spacer 21 depends on the thickness of the deposited layers 20, the thickness of the semiconductor layer 2, including the epitaxial layer 14 if present, the planarising dielectric layer 16 and on the spacer over-etch time. By offsetting the top of the fin 18 by at least partially removing the dummy fin 19 process latitude is created to free the sides of the fin 17 from the spacer material 20 and still have spacers 21 formed against the sides of the cavity.

[0042] If replacement gate transistors are to be formed, the complete dummy gate 9 of these replacement gate transistors is now selectively removed to ex-

pose the unpatterned semiconductor layer 2 in between the source 6 and drain 7 region.

[0043] Figures 6a and 6b shows the cross sections of the invertor circuit after forming the inside spacers 20 for dual gate transistors. Figures 7a and 7b shows the cross sections of the invertor circuit for triple gate transistors after forming the inside spacers 21. In this case the dummy gate stack 19 is completely removed from the semiconductor fin 17.

[0044] After forming the doped source 6, the doped drain 7 and defining the semiconductor fin 17 in the same layer 2 of semiconductor material of the insulated active area region 4 and covering the surfaces of the source and drain regions with dielectric layers 16 and sidewall spacers 21, the final gate stack is formed. This gate stack is used for both the FinFET devices according to the present invention as well as for the replacement gate devices. First the gate dielectric 22 is formed at least on the exposed surfaces of the semiconductor fin 17 and of the exposed surface of the unpatterned semiconductor layer 2 in case of the replacement gate device. This gate dielectric 22 can be an oxide, formed by thermal oxidation of the exposed semiconductor material. High-k materials allowing a small equivalent-oxide-thickness (EOT) for thicker layers can also be applied. Such layers can be deposited over the surface of the substrate or selectively formed on the exposed surfaces of the semiconductor fin 17, e.g. by atomic layer CVD. Then conductive material 23 is deposited, typically to conformally cover the surface of the substrate 1, to form, after patterning, the gate electrode 24. The workfunction of this conductive material 23 must be selected or modified to yield the desired threshold voltage of the FinFET. Polycrystalline silicon can be used and its workfunction can be modified by incorporating the desired amount and type of dopants such as B, P, As, Sb, or by adding alloys such as Ge. Metals can be applied as gate electrode material if these metals posses the desired workfunction. In case CMOS devices are formed appropriate metals are to be selected to form respectively the nMOS and the pMOS gate electrode. Midgap metals can be used to serve as gate electrode for both the nMOS and the pMOS transistor. The invention allows the use of high-k dielectrics and/or metal gates as the insulating layer 16 is only removed in those areas 8 where these high-k dielectrics 22 and/or metals 23 should be applied whereas the other regions remains protected by this layer 16. In this embodiment the cavity, formed in the planarizing dielectric 14 and in the semiconductor layer 2 by patterning the dummy gate 9 and the underlying semiconductor layer 2, is filled with the stack of gate dielectric 22 and gate electrode material 23.

[0045] If no gate dielectric 22 is present and the gate electrode 24 is directly contacting the semiconductor fin 17 a planar BiCMOS device instead of a CMOS device can be formed. The source 6 and drain 7 region are then used as emitter and collector regions while the gate electrode 24 acts as base electrode.

[0046] The gate of the FinFET is then defined by patterning the gate electrode material 23 in such a way that the gate electrode 24 extends over the cavity 25. This T-shaped gate electrode 24 will overlap the source 6 and drain 7 regions, but by selecting an appropriate thickness for the planarizing dielectric layer 14 the parasitic capacitance between the gate electrode 24 and the source 6 and drain 7 regions is kept low compared to the capacitance of the gate dielectric 21. Figures 8a and 8b show the cross section of the invertor circuit for triple gate transistors with a T-shaped gate electrode using oxide as gate dielectric 22.

[0047] Alternatively chemical-mechanical-polishing (CMP) can be used to locally remove the gate electrode material 23 and to create a gate electrode 24. In case high-k gate dielectrics 21 and/or metals 23 are used, CMP is applied to planarize the substrate surface and to remove at least the gate electrode material 23 outside the cavity 25 in the planarizing dielectric layer 16. Figures 9a and 9b show the cross section of the invertor circuit for triple gate transistors using oxide as gate dielectric 22 when gate electrode material 23 is polished down to the insulating dielectric 16.

[0048] In a preferred embodiment the semiconductor fin 17 was not doped. Optionally an high temperature anneal step can be given to diffuse dopants out of the doped source 6 and drain 7 regions into the semiconductor fin 17. The dopant diffusion into the semiconductor fin 17 is preferably limited to the region underneath the inside spacer 21 on top of the semiconductor fin 17 and should essentially not diffuse in the channel region 26 of the fin. Figure 7b shows for the pMOS device 41 the channel region 26 having a length "l" located in between the sidewall spacers 21 on top of the semiconductor fin 17. The thus doped part of the semiconductor fin 17 forms a good conductive connection between the channel part 26 of the transistor and the source 6 and drain 7 regions resulting in a lower overall series resistance if the transistor. This high temperature anneal step can be a separate step, but preferably this high temperature anneal step also activates the dopants incorporated in all semiconductor elements of the device or circuit. In case of a metal 23 or high-k dielectric 22 this anneal step is given prior to the deposition of the metal 23 or high-k dielectric gate 21 whatever comes first. If a semiconductor material is used as gate material 23 is formed, this outdiffusion step can be done after the deposition and doping of the semiconductor gate. The diffusion of dopants into the semiconductor fin 17 is also needed to compensate for the offset between source 6 and drain 7 regions and channel area 26. Fine-tuning of the source/drain and well implantations, and anneal conditions is needed in order to provide sufficient outdiffusion and avoid misalignment between the channel 26 and the source 6 and drain 7 areas. The process sequence according to the present invention is a gate last process. Additional process steps can be performed

such as additional local manipulation and modification of at least of the channel part 26 of the semiconductor fin 17. Examples of such extra local processing are incorporating of Ge in the channel region 26 or nitridation of the channel region to prevent outdiffusion of dopants from underneath the spacers 21 into the channel region 26.

[0049] A standard back-end-of-line (BEOL) processing will complete the processing. This BEOL process comprises the steps of forming insulating layers, defining vias and trenches in these insulating layers to contact underlying devices and interconnect levels, filing these vias and trenches with conductive materials to obtain the desired interconnect scheme. A person skilled in the art knows this part of a CMOS process flow and the various alternatives, such as dual damascene processing.

Claims

1. A method for forming a FinFET comprising the steps of:
   - providing a substrate (1), comprising a semiconductor layer (2),
   - forming in said semiconductor layer (2) active areas (4) insulated from each other by field areas (5),
   - forming within at least one of said active areas (4) on said semiconductor layer (2) at least one dummy gate (9),
   - forming, within said at least one of said active areas (4) and self aligned to said dummy gate (9), source (6) and drain (7) regions in said semiconductor layer (2),
   - covering said substrate (1) with an insulating layer (16) leaving said dummy gate (9) exposed,
   - forming an open cavity (25) in said insulating layer (16) and in said semiconductor layer (2) by patterning said dummy gate (9) and said semiconductor layer (2) to form respectively a dummy fin (19) and a semiconductor fin (17) aligned to said dummy fin (19), both fins (17), (19) extending from the source (6) to the drain (7) of said at least one active area (4), thereby exposing said semiconductor layer (2)

2. A method as recited in claim 1 wherein said step of forming an open cavity (25) comprises the steps of first patterning said dummy gate (9) to form said dummy fin (19) and then patterning, self aligned to said dummy fin (19), said semiconductor layer (2) to form said semiconductor fin (17).

3. A method as recited in claim 1 or 2 further comprising the steps of:
   - reducing the thickness of said dummy fin (19),
   - forming spacers (21) against the sidewalls of said cavity at the source (6), drain (7) and field (5) side, and
   - forming a gate dielectric (22) and a gate electrode (24) overlapping said semiconductor fin (17).

4. A method as recited in claim 3 wherein, the step of providing a substrate (1) comprising a semiconductor layer (2) comprises the step of forming, at least within said at least one of said active areas (4), a dielectric layer (3) separating semiconductor layer (2) from said substrate (1).

5. A method as recited in claim 4 wherein said substrate (1) is a silicon-on-insulator wafer.

6. A method as recited in claim 5 wherein the step of covering said substrate (1) with an insulating layer (16) leaving said dummy gate (9) exposed, comprises the steps of:
   - forming on said substrate (1) said insulating layer (16), and
   - planarizing said insulating layer (16) until said dummy gate (9) is exposed.

7. A method as recited in claim 6 wherein said dummy fin (19) consists of a stack of layers (10,12, 13) selectively removable to each other.

8. A method as recited in claim 7 wherein the step of reducing the thickness of said dummy fin. (19), comprises the step of removing at least one layer (13) of said stack of layers (10,12,13).

9. A method as recited in claim 8 further comprising the step of removing the remaining layers (10, 12) of said stack of layers (10,12,13).

10. A method as recited in claim 8 or 9 wherein of the step of forming a gate dielectric (22) and gate electrode (24) overlapping said semiconductor fin (17), comprises the steps of:
    - depositing a layer of a gate dielectric and a layer of a gate electrode (23) material on said substrate (1);
    - planarizing said layer of a gate dielectric and said layer of a gate electrode material until said insulating layer (16) is exposed.

11. A method as recited in claim 10 wherein the step of forming a gate dielectric (22) and gate electrode (24) overlapping said semiconductor fin (17), comprises the steps of:

- depositing a layer of a gate dielectric and a layer of gate electrode material (23) on said substrate (1), and;
- patterning said layer of gate dielectric and said layer of gate electrode material to form a gate dielectric (22) and a gate electrode (24) overlapping said cavity (25).

12. A method as recited in claim 10 or 11 wherein said layer of a gate dielectric comprises a layer of a high-k dielectric.

13. A method as recited in claim 10 or 11 wherein said layer of a gate electrode material comprises a metal layer.

14. A method as recited in any one of the preceding claims further comprising the step of forming at least one planar FET device on an active area (4) other than said at least one of said active areas (4).

15. A method as recited in claim 14 wherein the step of forming at least one dummy gate (9), comprises the steps of:

- depositing a stack of a dielectric layer (10) and a conductor layer (12), and
- patterning said stack of layers to form at least one dummy gate (9).

16. A method as recited in claim 15 wherein the step of patterning said stack of layers (10, 12) to form at least one dummy gate (9), comprises the step of forming the gate of said planar FET device.

17. A CMOS circuit, comprising:

- at least two active areas (4) formed in a semiconductor layer (2), said at least two active areas (4) insulated from each other by field regions (5),
- each active area comprising at least one FinFET device (40,41),
- each of said at least one FinFET devices (40,41) comprising a source (6) and a drain (7) formed in said semiconductor layer (2), and a cavity ((25)) in between, with a semiconductor fin (17) formed in said semiconductor layer (2) and extending in said cavity (25) from said source (6) to said drain (7).

18. A CMOS circuit as recited in claim 17 further comprising:

- an insulating oxide (16) covering said CMOS circuit outside said cavity (25) , and
- spacers (21) formed against the inner sidewalls of said cavity (25).

19. A CMOS circuit as recited in claim 18 further comprising a stack of a gate dielectric (22) and a gate electrode (24) overlapping said semiconductor fin (17).

20. A CMOS circuit as recited in claim 19 wherein said gate dielectric (22) comprises a high-k dielectric.

21. A CMOS circuit as recited in claim 19 wherein said gate electrode (24) comprises a metal.

22. A CMOS circuit as recited in claims 19 wherein said stack of a gate dielectric (22) and a gate electrode (24) extends beyond said cavity (25).

23. A CMOS circuit as recited in claims 19 wherein said stack of a gate dielectric (22) and a gate electrode (24) is coplanar with said insulating oxide (16).

24. A CMOS circuit as recited in all foregoing claims further comprising at least one active area comprising at least one planar FET device.

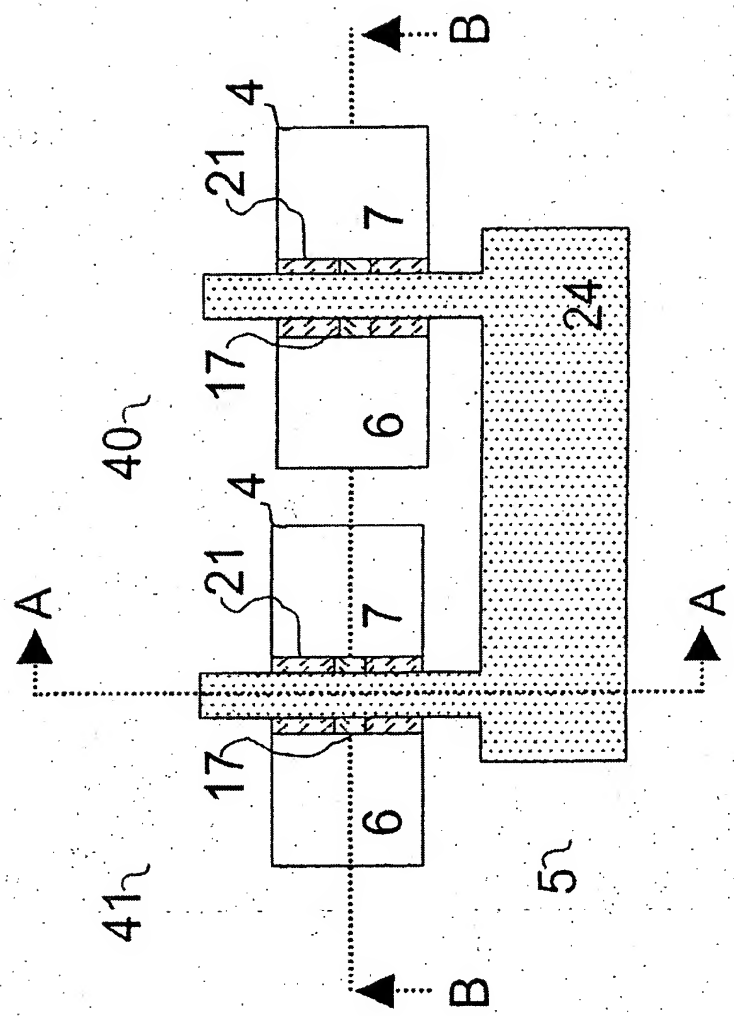
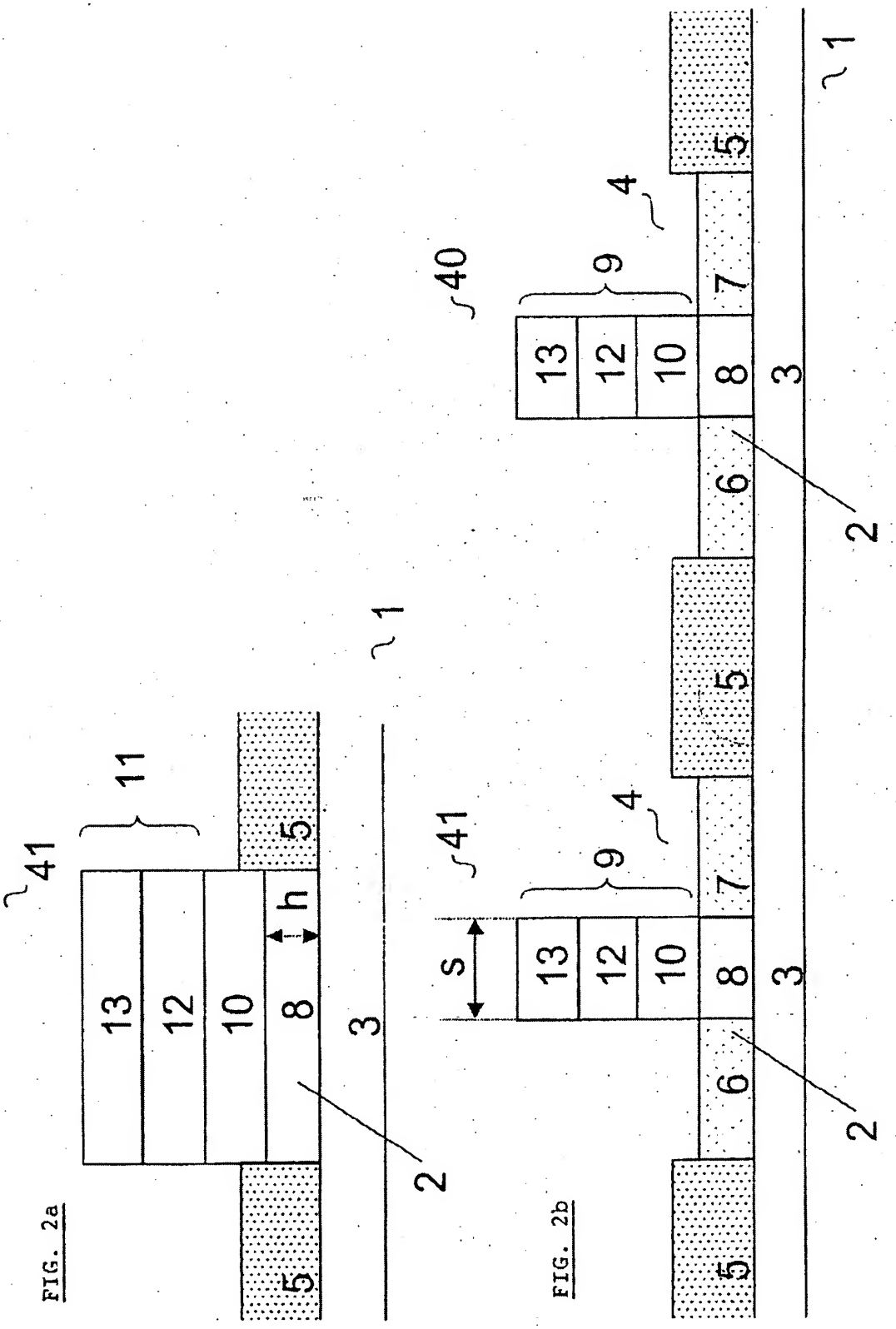


FIG. 1



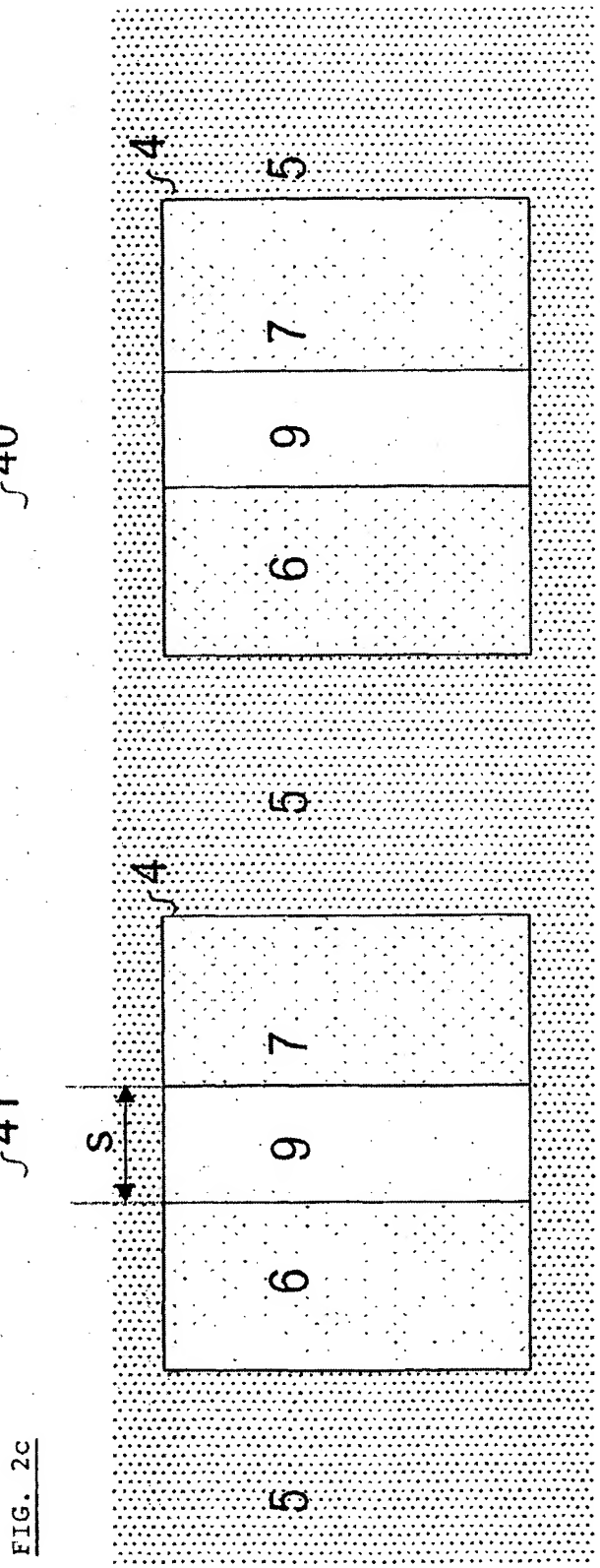


FIG. 2c

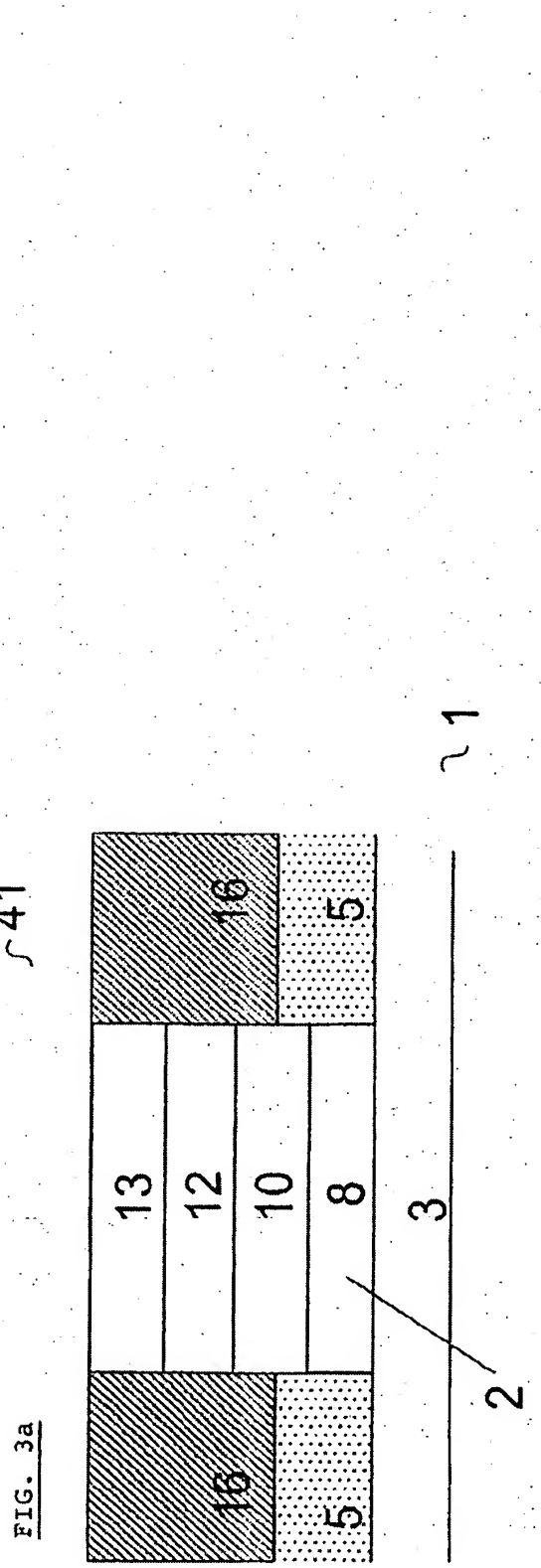


FIG. 3a

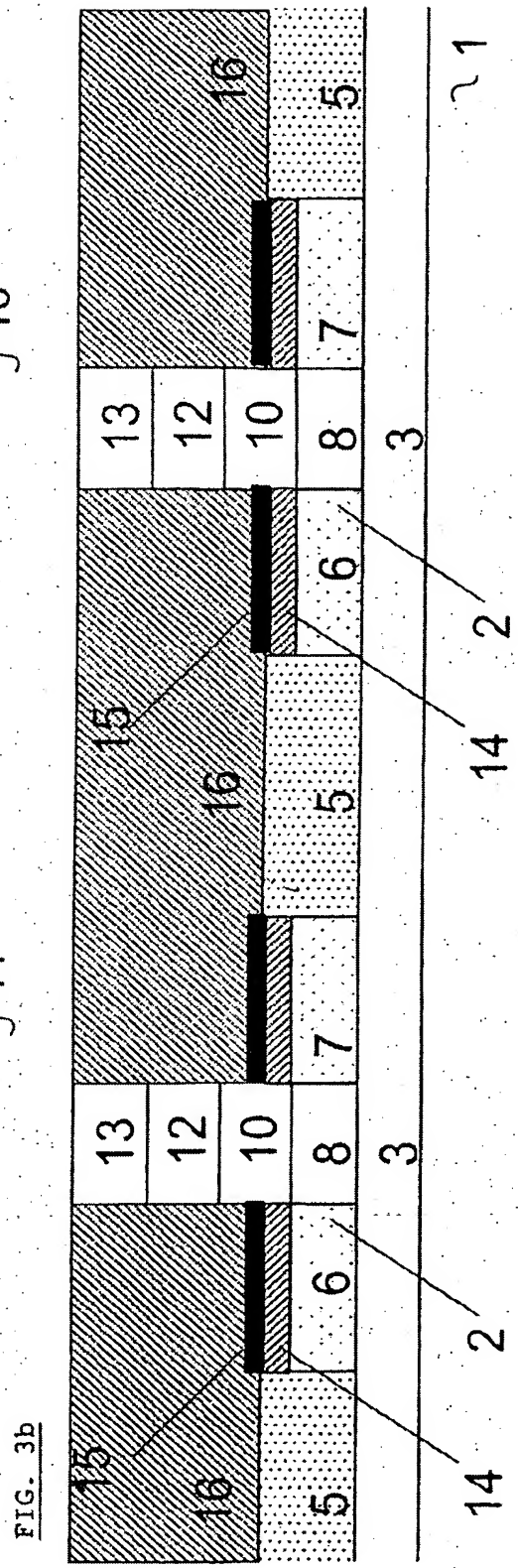


FIG. 3b

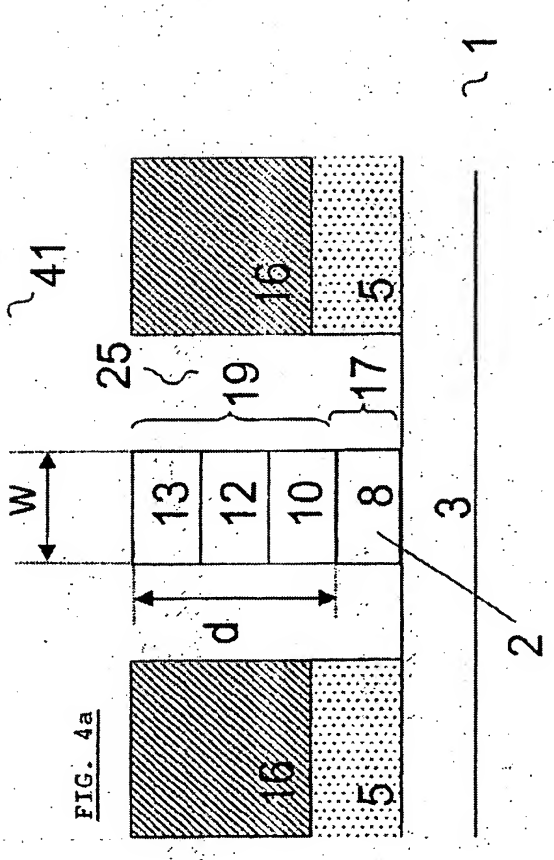

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FIG. 4a

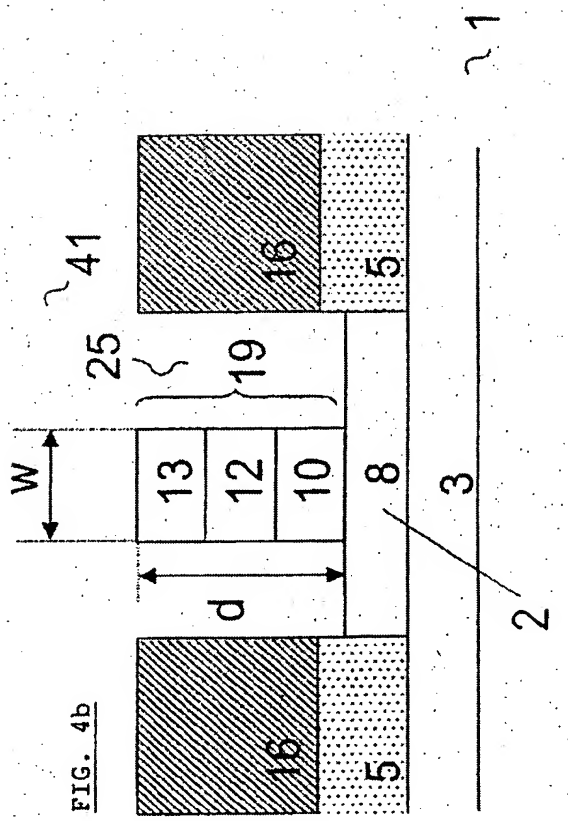
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FIG. 4b

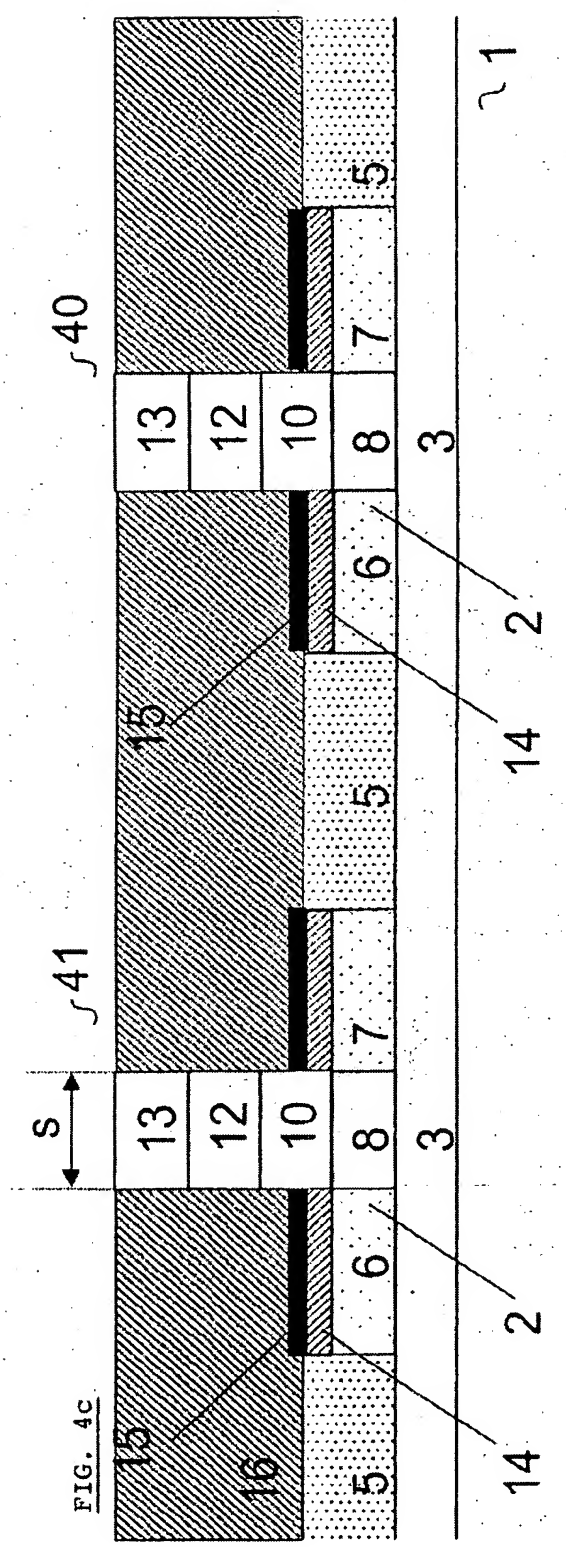


FIG. 4c

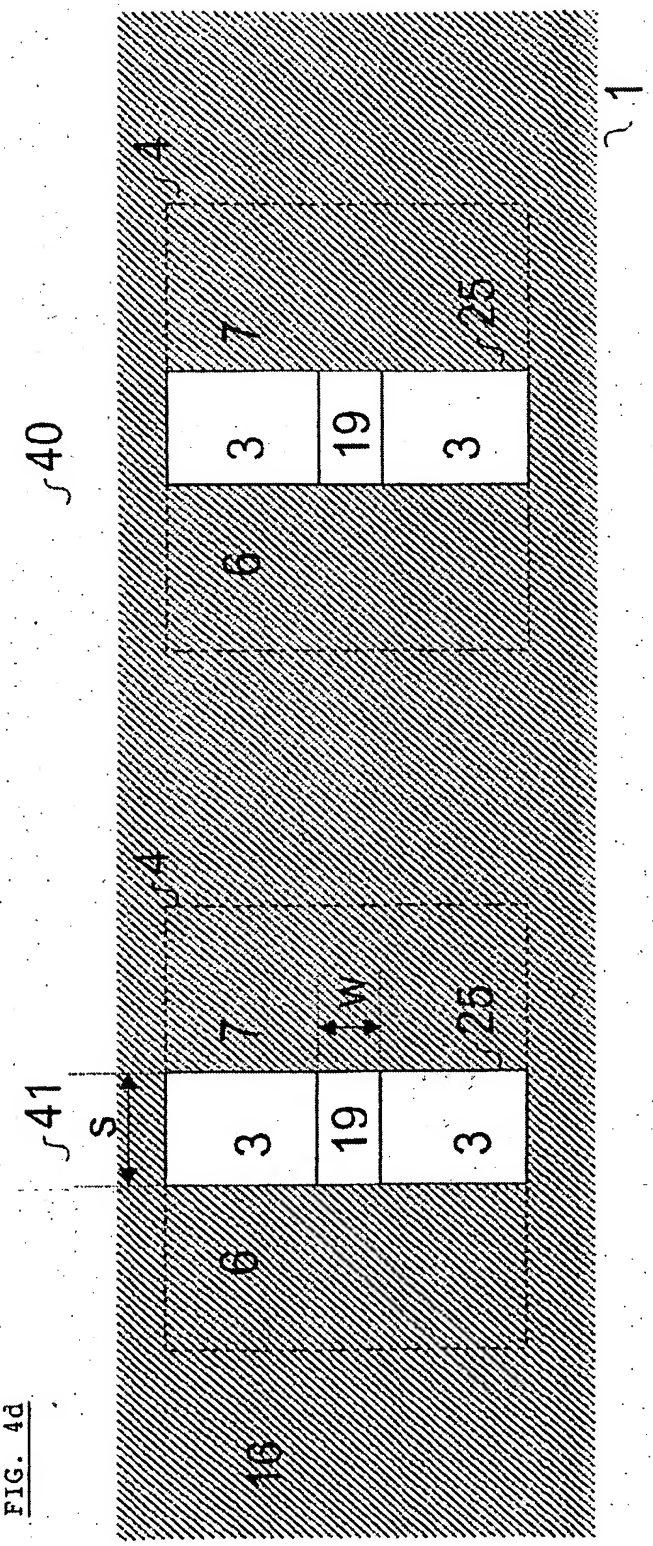


FIG. 4d

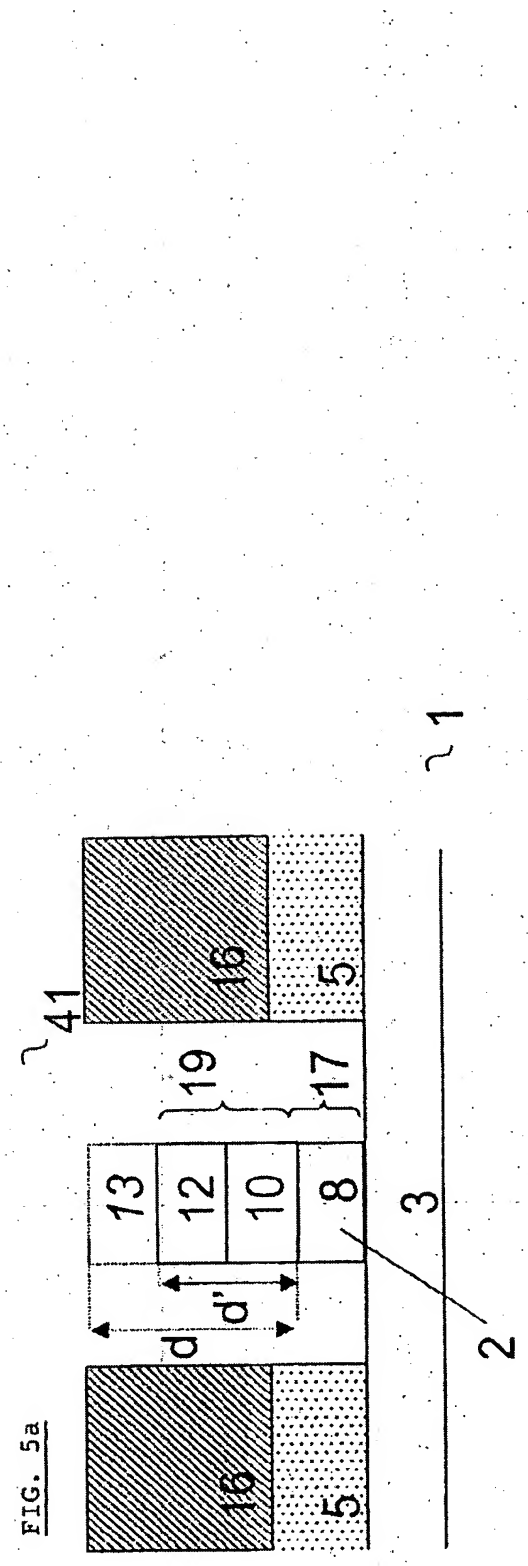


FIG. 5a

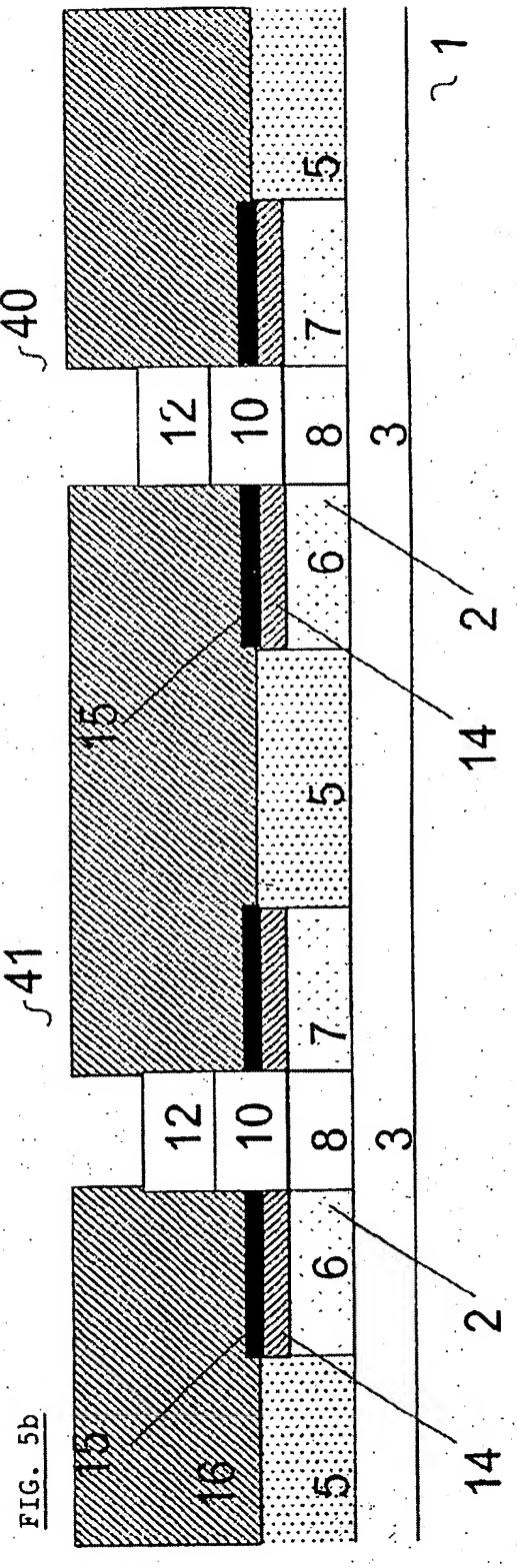
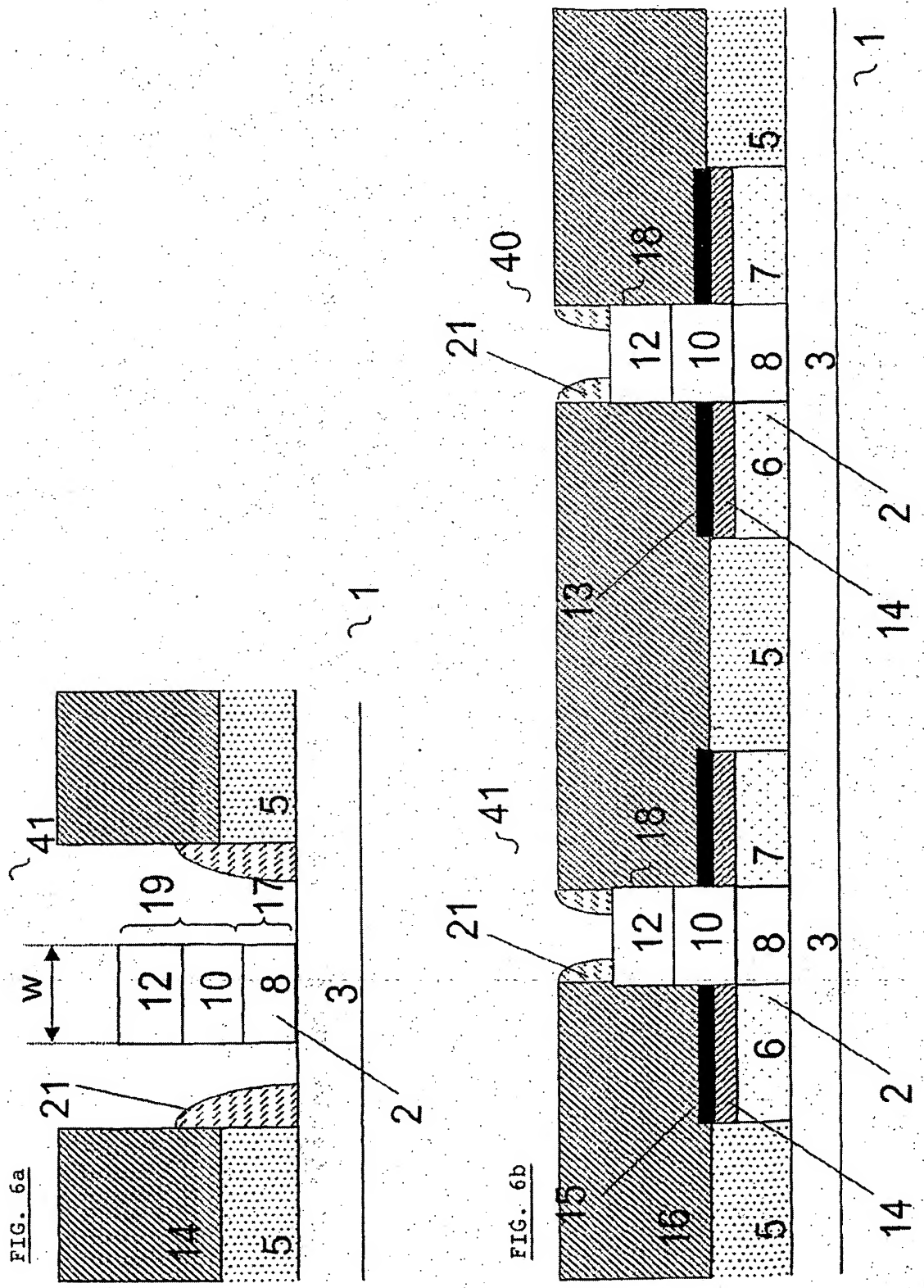


FIG. 5b



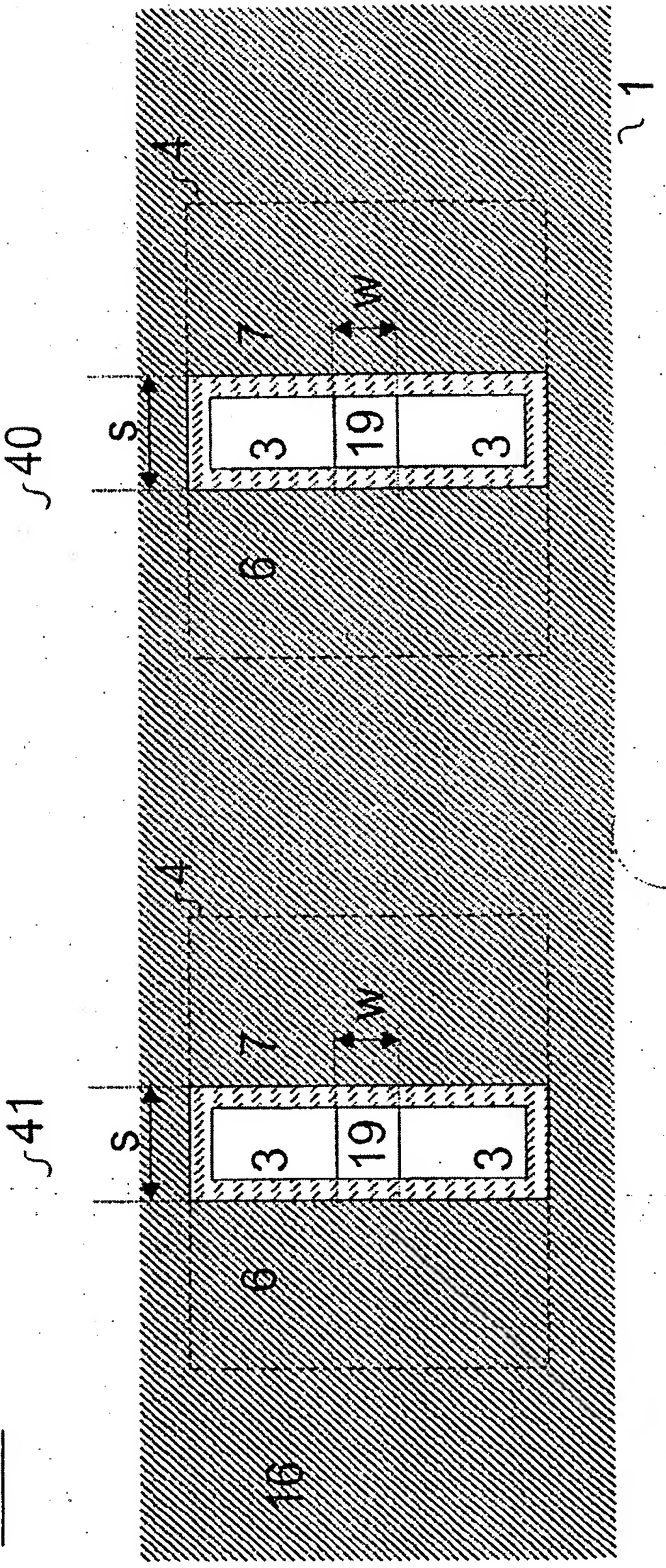


FIG. 6c

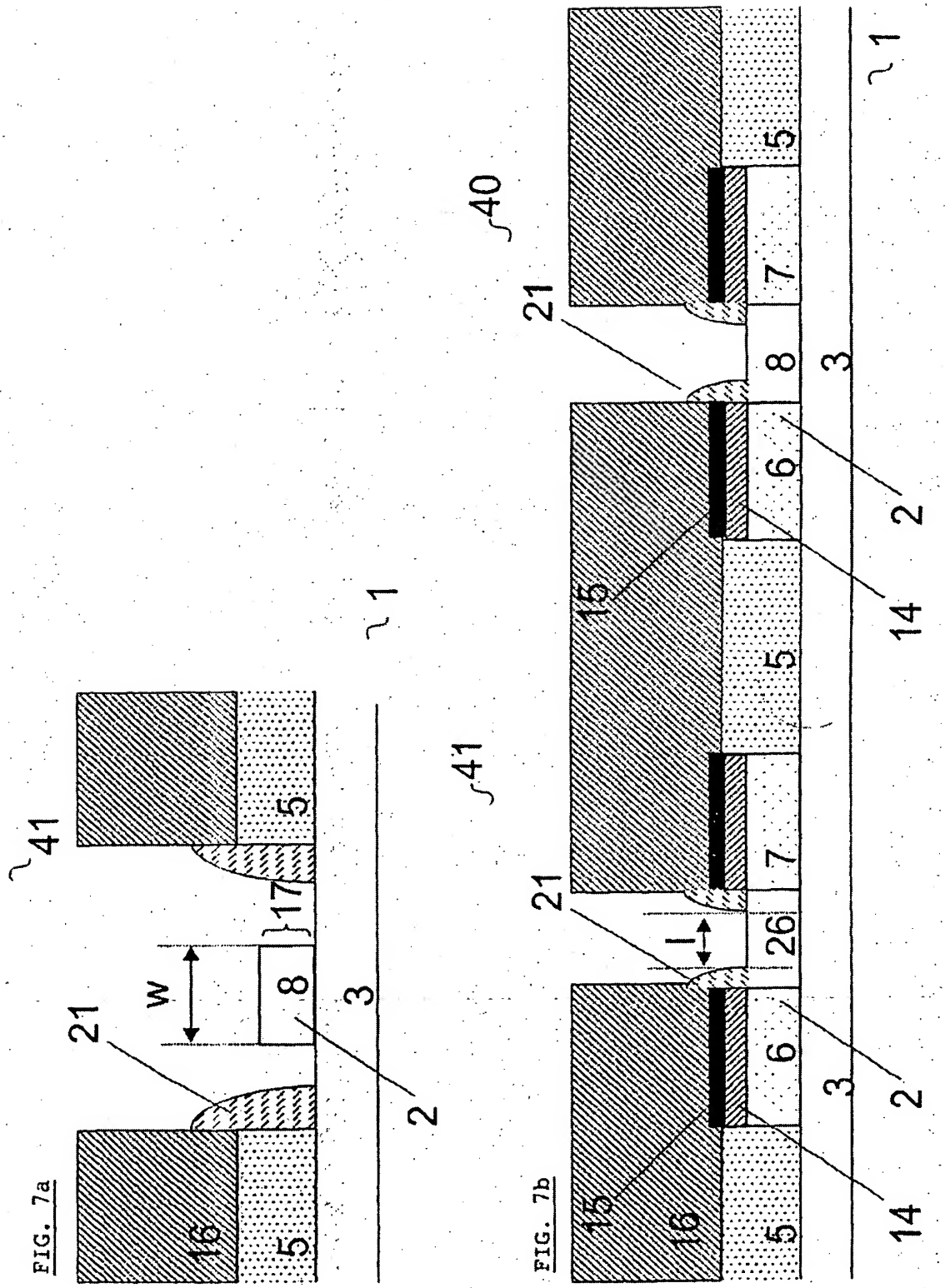

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FIG. 7a
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FIG. 7b

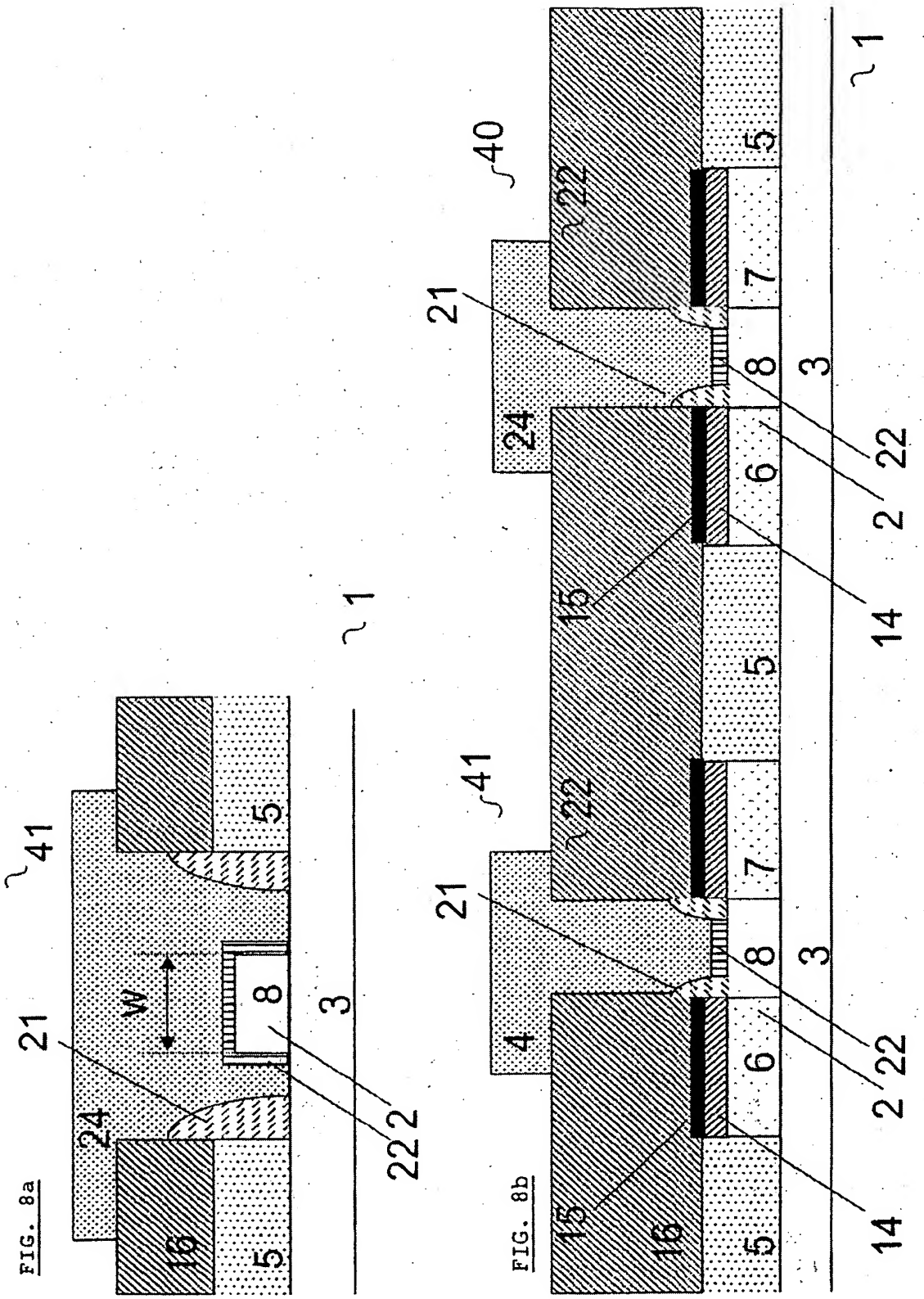
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FIG. 8a
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FIG. 8b

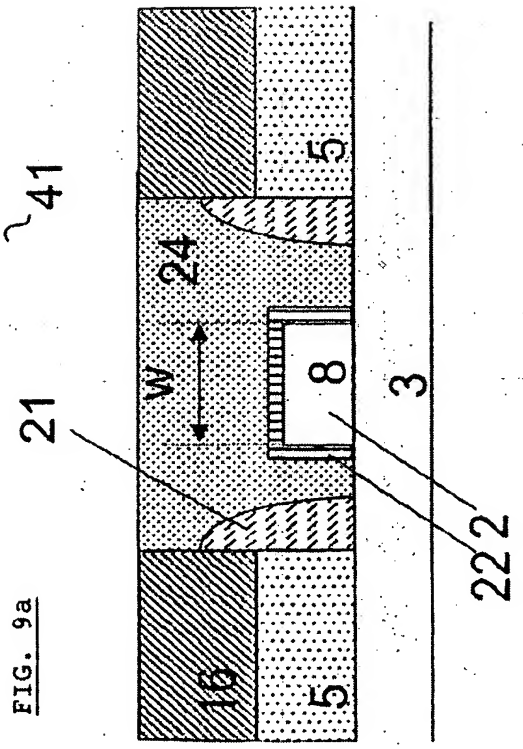

FIG. 9a

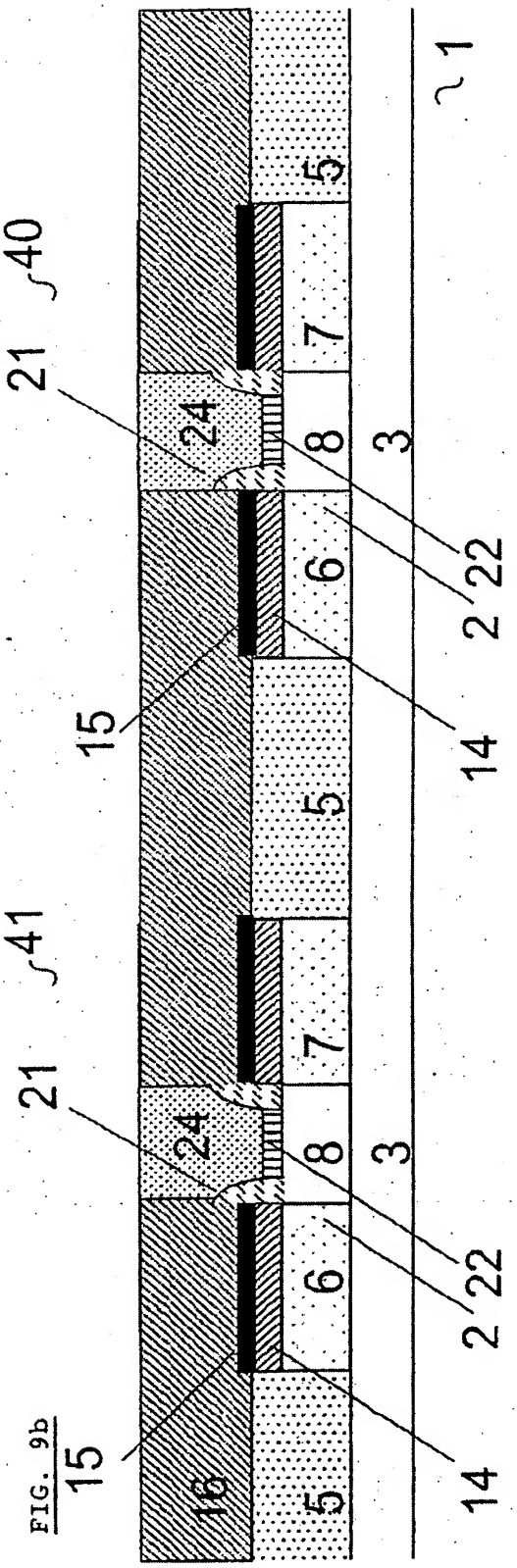

FIG. 9b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 44 7135

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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Y	* column 3, line 6 - line 65; figure 8 * * column 4, line 40 - column 6, line 12; figures 12-17 * ---	3-11,13, 15	
X	HUANG X ET AL: "SUB-50 NM P-CHANNEL FINFET" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE INC. NEW YORK, US, vol. 48, no. 5, May 2001 (2001-05), pages 880-886, XP001099716 ISSN: 0018-9383	17	
Y	* page 881, left-hand column - page 882, left-hand column; figures 1-4 * ---	3-11,13, 15	
X	CHOI Y-K ET AL: "NANOSCALE CMOS SPACER FINFET FOR THE TERABIT ERA" IEEE ELECTRON DEVICE LETTERS, IEEE INC. NEW YORK, US, vol. 23, no. 1, January 2002 (2002-01), pages 25-27, XP001112379 ISSN: 0741-3106	17,24	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
A	* page 25, right-hand column - page 26, right-hand column; figures 1,2 * ---	1-16, 18-23	
D,X	HISAMOTO D ET AL: "FOLDED-CHANNEL MOSFET FOR DEEP-SUB-TENTH MICRON ERA" INTERNATIONAL ELECTRON DEVICES MEETING 1998. IEDM TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 6 - 9, 1998, NEW YORK, NY: IEEE, US, 6 December 1998 (1998-12-06), pages 1032-1034, XP000859545 ISBN: 0-7803-4775-7 * the whole document * -----	1-5	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	17 December 2002	Agne, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82